

**AMENDMENTS TO THE CLAIMS**

Claim 1 (currently amended): A semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region having a drain terminal in a well formed in a semiconductor layer, and a gate terminal fabricated atop a channel region which receives a first input signal, wherein the channel region is formed between said source region and drain region and a gate electrode receives the first input signal to influence the channel region through a gate insulating film, wherein:

each of said semiconductor elements is electrically separated from the others;

said well in each of said semiconductor elements is provided with a substrate terminal which receives a second input signal through a contact hole formed therein at a region other than said source region and drain region; and

~~the first and second input signals are different signals that are synchronized with each other~~  
each of the first and second input signals is any given binary signal provided externally as user data.

Claim 2 (original): The semiconductor device of Claim 1, wherein operating characteristics are changed by adjusting impurity concentration in said channel region and levels of a high voltage and a low voltage applied to said gate terminal and substrate terminal.

Claim 3 (original): The semiconductor device of Claim 1, wherein said semiconductor layer in each of said semiconductor elements is electrically separated from each other by means of an oxide film.

Claim 4 (withdrawn): A semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region

having a drain terminal in a well formed in a semiconductor layer, and a gate terminal fabricated on a channel region, formed between said source region and drain region, through a gate insulating film, wherein:

each of said semiconductor elements is electrically separated from the others;

said semiconductor layer is composed of a shallow well region, a heavily doped region for reducing resistance of said shallow well region, and a deep well region, which are sequentially layered in a vertical direction; and

said semiconductor layer is provided with a substrate terminal through a contact hole at a region other than said source region and drain region.

Claim 5 (withdrawn): The semiconductor device of Claim 4, wherein:

each of said semiconductor elements is electrically separated from the others by means of a separation region; and

a depth of said separation region is set at least as large as a sum of a depth of said shallow well region and a width of a depletion layer formed at a junction of said shallow well region and deep well region.

Claim 6 (previously presented): The semiconductor device of Claim 1, wherein:

the semiconductor elements are organized into pairs of semiconductor elements, each pair of semiconductor elements including a P-type semiconductor element and an N-type semiconductor element;

for each pair of semiconductor elements,

a high potential is supplied to a source terminal of said P-type semiconductor element and a low potential is supplied to a source terminal of said N-type semiconductor element;

a gate terminal of said P-type semiconductor element is connected to a gate terminal of said N-type semiconductor element thereby to form the first input terminal;

a substrate terminal of said P-type semiconductor element is connected to a substrate terminal of said N-type semiconductor element, thereby to form the second input terminal; and

a drain terminal of said P-type semiconductor element is connected to a drain terminal of said N-type semiconductor element, thereby to form an output terminal.

Claim 7 (withdrawn): The semiconductor device of Claim 4, wherein:

each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type semiconductor element;

a high potential is supplied to a source terminal of said P-type semiconductor element and a low potential is supplied to a source terminal of said N-type semiconductor element;

gate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a first input terminal;

substrate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a second input terminal; and

drain terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

Claim 8 (original): The semiconductor device of Claim 6, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

Claim 9 (withdrawn): The semiconductor device of Claim 7, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

Claim 10 (previously presented): A semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region having a drain terminal in a well formed in a semiconductor layer, and a gate terminal fabricated atop a channel region, formed between said source region and drain region, with a gate insulating film between the gate terminal and the channel region, wherein:

each of said semiconductor elements is electrically separated from the others;

said well in each of said semiconductor elements is provided with a substrate terminal through a contact hole formed therein at a region other than said source region and drain region;

the semiconductor elements are organized into pairs of semiconductor elements, each pair of semiconductor elements including a P-type semiconductor element and an N-type semiconductor element;

for each pair of semiconductor elements,

a high potential is supplied to a source terminal of said P-type semiconductor element and a low potential is supplied to a source terminal of said N-type semiconductor element;

a gate terminal of said P-type semiconductor element and a substrate terminal of said N-type semiconductor element are connected to each other, thereby to form a first input terminal;

a gate terminal of said N-type semiconductor element and a substrate terminal of said P-type semiconductor element are connected to each other, thereby to form a second input terminal;  
and

a drain terminal of said P-type semiconductor element is connected to a drain terminal of said N-type semiconductor element thereby to form an output terminal.

Claim 11 (withdrawn): The semiconductor device of Claim 4, wherein:

each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type semiconductor element;

a high potential is supplied to a source terminal of said P-type semiconductor element and a low potential is supplied to a source terminal of said N-type semiconductor element;

a gate terminal of said P-type semiconductor element and a substrate terminal of said N-type semiconductor element are connected to each other, thereby to form a first input terminal;

a gate terminal of said N-type semiconductor element and a substrate terminal of said P-type semiconductor element are connected to each other, thereby to form a second input terminal; and

drain terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

Claim 12 (original): The semiconductor device of Claim 10, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said first input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said high potential.

Claim 13 (withdrawn): The semiconductor device of Claim 11, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said first input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said high potential.

Claim 14 (original): The semiconductor device of Claim 6, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said low potential and lower than said high potential when said second input terminal is supplied with said low potential, and lower than said low potential when said second input terminal is supplied with said high potential.

Claim 15 (withdrawn): The semiconductor device of Claim 7, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said low potential and lower than said high potential when said second input terminal is supplied with said low potential, and lower than said low potential when said second input terminal is supplied with said high potential.

Claim 16 (original): The semiconductor device of Claim 10, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said second input terminal is supplied with said high

potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said low potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said first input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said low potential.

Claim 17 (withdrawn): The semiconductor device of Claim 11, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said second input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said low potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said first input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said low potential.

Claim 18 (previously presented): A semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region having a drain terminal in a well formed in a semiconductor layer, and a gate terminal fabricated atop a channel region, formed between said source region and drain region, with a gate insulating film between the gate terminal and the channel region, wherein:

each of said semiconductor elements is electrically separated from the others;

said well in each of said semiconductor elements is provided with a substrate terminal through a contact hole formed therein at a region other than said source region and drain region;

the semiconductor elements are organized into pairs of semiconductor elements, each pair of semiconductor elements including a P-type semiconductor element and an N-type semiconductor element;

for each pair of semiconductor elements,

a drain terminal of said N-type semiconductor element is supplied with a high potential and a drain terminal of said P-type semiconductor element is supplied with a low potential;

a gate terminal of said P-type semiconductor element is connected to a gate terminal of said N-type semiconductor element, thereby to form a first input terminal;

a substrate terminal of said P-type semiconductor element is connected to a substrate terminal of said N-type semiconductor element, thereby to form a second input terminal; and

a source terminal of said P-type semiconductor element is connected to a source terminal of said N-type semiconductor element, thereby to form an output terminal.

Claim 19 (withdrawn): The semiconductor device of Claim 4, wherein:

each of said semiconductor elements is composed of a pair of a P-type semiconductor element and an N-type semiconductor element;

a drain terminal of said N-type semiconductor element is supplied with a high potential and a drain terminal of said P-type semiconductor element is supplied with a low potential;

gate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a first input terminal;

substrate terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form a second input terminal; and

source terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.



Claim 20 (original): The semiconductor device of Claim 18, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

Claim 21 (withdrawn): The semiconductor device of Claim 19, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

Claim 22 (currently amended): A The semiconductor device of Claim 1, comprising a plurality of semiconductor elements, each being provided with a source region having a source terminal and a drain region having a drain terminal in a well formed in a semiconductor layer, and a gate terminal fabricated atop a channel region which receives a first input signal, wherein the channel region is formed between said source region and drain region and a gate electrode receives the first input signal to influence the channel region through a gate insulating film, wherein:  
each of said semiconductor elements is electrically separated from the others;  
said well in each of said semiconductor elements is provided with a substrate terminal which receives a second input signal through a contact hole formed therein at a region other than said source region and drain region; and  
the first and second input signals are different signals that are synchronized with each other,  
wherein:

the semiconductor elements are organized into pairs of semiconductor elements, each pair of semiconductor elements including a P-type semiconductor element and an N-type semiconductor element;

for each pair of semiconductor elements,

a high potential is supplied to a drain terminal of said N-type semiconductor element and a low potential is supplied to a drain terminal of said P-type semiconductor element;

a gate terminal of said N-type semiconductor element is connected to a substrate terminal of said P-type semiconductor element, thereby to form the first input terminal;

a gate terminal of said P-type semiconductor element is connected to a substrate terminal of said N-type semiconductor element ~~are connected to each other~~, thereby to form the second input terminal; and

a source terminal of said P-type semiconductor element is connected to a source terminal of said N-type semiconductor element, thereby to form an output terminal.

Claim 23 (withdrawn): The semiconductor device of Claim 4, wherein:

each of said semiconductor elements is composed of a P-type semiconductor element and an N-type semiconductor element;

a high potential is supplied to a drain terminal of said N-type semiconductor element and a low potential is supplied to a drain terminal of said P-type semiconductor element;

a gate terminal of said N-type semiconductor element and a substrate terminal of said P-type semiconductor element are connected to each other, thereby to form a first input terminal;

a gate terminal of said P-type semiconductor element and a substrate terminal of said N-type semiconductor element are connected to each other, thereby to form a second input terminal; and

drain terminals of said P-type semiconductor element and N-type semiconductor element are connected to each other, thereby to form an output terminal.

Claim 24 (original): The semiconductor device of Claim 22, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said first input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said high potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

Claim 25 (withdrawn): The semiconductor device of Claim 23, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said first input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said high potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said high potential when said second input terminal is supplied with said low potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said high potential.

Claim 26 (original): The semiconductor device of Claim 18, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said low potential and lower than said high potential when

said second input terminal is supplied with said low potential, and lower than said low potential when said second input terminal is supplied with said high potential.

Claim 27 (withdrawn): The semiconductor device of Claim 19, wherein each of said P-type semiconductor element and N-type semiconductor element is arranged in such a manner that a threshold voltage becomes higher than said low potential and lower than said high potential when said second input terminal is supplied with said low potential, and lower than said low potential when said second input terminal is supplied with said high potential.

Claim 28 (original): The semiconductor device of Claim 22, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said first input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said low potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said second input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said second input terminal is supplied with said low potential.

Claim 29 (withdrawn): The semiconductor device of Claim 23, wherein:

said P-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said first input terminal is supplied with said high potential, and lower than said high potential and higher than said low potential when said first input terminal is supplied with said low potential; and

said N-type semiconductor element is arranged in such a manner that a threshold voltage becomes lower than said low potential when said second input terminal is supplied with said high potential and lower than said high potential and higher than said low potential when said second input terminal is supplied with said low potential.

Claim 30 (withdrawn): A semiconductor device comprising:

a semiconductor substrate;

a background insulating film formed over said semiconductor substrate;

a semiconductor layer of P- or N-type which is formed over said background insulating film and made into a first electrode, each element in said semiconductor layer being separated from an adjacent element by means of an insulating separation region which encircles each element;

a source region and a drain region which are formed in said semiconductor layer and made into a second electrode and a third electrode, respectively, a conduction type of each being opposite to a conduction type of said semiconductor layer;

a channel region formed between said source region and drain region;

a gate insulating film formed over said channel region; and

a gate electrode formed as a fourth electrode on said gate insulating film,

said semiconductor device being characterized in that said semiconductor layer is separated by means of said separation region, and a contact hole is formed through said each semiconductor layer separated by means of said separation region, at a region other than said source region and drain region.

Claim 31 (withdrawn): A semiconductor device comprising:

a semiconductor substrate;

a deep well region of P- or N-type formed in said semiconductor substrate;

a shallow well region which is formed over said deep well region and made into a first electrode, a conduction type of said shallow well region being opposite to a conduction type of said deep well region;

a source region and a drain region of P- or N-type which are formed in said shallow well region and made into a second electrode and a third electrode, respectively;

a channel region formed between said source region and drain region;

a gate insulating film formed over said channel region; and

a gate electrode formed as a fourth electrode on said gate insulating film,

said semiconductor device being characterized in that:

at least said shallow well region in each element is electrically separated from the shallow well region in an adjacent element by means of a separation region; and

a contact hole is provided to said shallow well region in each element separated from the shallow well region in the adjacent element by means of said separation region, at a region other than said source region and drain region.

Claim 32 (withdrawn): The semiconductor device of Claim 30 or 31, wherein:

the elements having opposite conduction types are paired off;

a source of a P-type semiconductor element is fixed at a high potential and a source of an N-type semiconductor element is fixed at a low potential;

gates of both said P-type semiconductor element and N-type semiconductor element form a first input terminal;

said contact holes in both said P-type semiconductor element and N-type semiconductor element form a second input terminal; and

drains of both said P-type semiconductor element and N-type semiconductor element form an output terminal.

Claim 33 (withdrawn): The semiconductor device of Claim 30 or 31, wherein:

- the elements having opposite conduction types are paired off;
- a source of a P-type semiconductor element is fixed at a high potential and a source of an N-type semiconductor element is fixed at a low potential;
- a gate of said P-type semiconductor element and said contact hole in said N-type semiconductor element form a first input terminal;
- both a gate of said N-type semiconductor element and said contact hole in said P-type semiconductor element form a second input terminal;
- drains of both said P-type semiconductor element and N-type semiconductor element form an output terminal.

Claim 34 (withdrawn): The semiconductor element of Claim 30 or 31, wherein:

- the elements having opposite conduction types are paired off;
- a drain of an N-type semiconductor element is fixed at a high potential and a drain of a P-type semiconductor element is fixed at a low potential;
- gates of both said N-type semiconductor element and P-type semiconductor element form a first input terminal;
- said contact holes in both said N-type semiconductor element and P-type semiconductor element form a second input terminal; and
- sources of both said N-type semiconductor element and P-type semiconductor element form an output terminal.

Claim 35 (withdrawn): The semiconductor element of Claim 30 or 31, wherein:

- the elements having opposite conduction types are paired off;

a drain of an N-type semiconductor element is fixed at a high potential and a drain of a P-type semiconductor element is fixed at a low potential;

both a gate of said N-type semiconductor element and said contact hole in said P-type semiconductor element form a first input terminal;

both a gate of said P-type semiconductor element and said contact hole in said N-type semiconductor element form a second input terminal; and

drains of both said P-type semiconductor element and N-type semiconductor element form an output terminal.

Claim 36 (withdrawn): A method of driving the semiconductor device in any of Claims 30 through 35 characterized in that said gate and said contact hole form separate input terminals, into which different input signals synchronized to each other are inputted respectively.

Claim 37 (new): The semiconductor device of Claim 1, wherein each of said semiconductor element is specified so that when a second input terminal is at low potential, a threshold voltage for the gate terminal is higher than high potential, and when the second input terminal is at the high potential, the threshold voltage for the gate terminal is higher than the low potential and lower than the high potential.

Claim 38 (new): The semiconductor device of Claim 1, wherein each of said semiconductor element is specified so that when a second input terminal is at low potential, a threshold voltage for the gate terminal is higher than low potential and lower than high potential, and when the second input terminal is at the high potential, the threshold voltage for the gate terminal is lower than the low potential.